

Appl. No. 10/665,654
Amdt. dated 1/3/2005
Reply to the Office Action of 10/01/2004

REMARKS/ARGUMENTS

Reexamination and reconsideration of this application as amended is requested. By this amendment, Claims 1 and 9-11 have been amended. After this amendment, Claims 1-14 remain pending in this application.

(2-4) Claim Rejections - 35 USC § 112

(2) The Examiner objected to Claim 8 because of minor informalities. Applicants have amended line 1 of Claim 8 to replace "claim2" with "claim 2".

In view of the amendment to Claim 8, Applicants believe that the objection to Claim 8, as discussed above, has been overcome. Applicants request that the Examiner withdraw the objection to Claim 8.

(3-4) The Examiner has rejected Claims 1-14 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

Applicants have amended independent Claims 1 and 9-10 to more clearly and affirmatively recite the present invention. Amended Claims 1, and 9-10 more clearly and affirmatively recite "a series of at least two delay stages" and "wherein when the input signal to be delayed is in a low state, each transistor of the first conductivity type is active and each transistor of the second conductivity type is inactive; and wherein when the input signal to be delayed is in a high state, each transistor of the first conductivity type is inactive and each transistor of the second conductivity type is active". Claim 11 has also been similarly amended. Support for this amendment may be found in the specification as originally filed, see for example FIG. 3; pages 6-7. No new matter has been added.

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Claims 2-8, and 12-14 depend from Claims 1 and 11 respectively, either directly or by way of an intervening claim, and since dependent claims recite all of the limitations of the independent claim; the Applicants submit that claims 2-8, and 12-14 are also allowable, and the Examiner's rejection under 35 U.S.C. § 112, second paragraph should be withdrawn.

(5-6) Rejections - 35 USC § 102

(5-6) The Examiner rejected Claims 1, 3, 9 and 10 under 35 U.S.C. 102(b) as being anticipated by Lee (U.S. Patent No. 5,157,279). This rejection is respectfully traversed.

Lee teaches a data output driver of a semiconductor memory device that produces a high output gain. First and second output transistors receive at each gate a pair of signals having logic levels complementary to each other. The data output driver is provided with an input line that is connected to the gate of the first output transistor. A pull-up transistor has a gate connected to the input line and has a channel connected in between the power source voltage terminal and a bulk of the first output transistor. A pull-down transistor has a gate connected to the input line and has a channel connected in between the bulk and the ground voltage. Lee also teaches that the data output driver includes a bias device that is connected in between the input line and ground voltage. The bias device supplies a given bias voltage to the input line when the potential of the input line is lower than the given voltage level. (See Col. 2, Lines 54-68 and Col. 3, Lines 1-4).

Lee teaches that the pull-up and pull-down transistors are made up of NMOS transistors. The pull-down transistor is made to receive the potential of the input line through an inverter. The bias device also includes an NMOS transistor. When the data is in logic "low" state, that is, a ground voltage level, the first NMOS transistor turns off and the second NMOS transistor turns on and the output node drops to a logic "low" state. The pull-up transistor turns off and the pull-down transistor turns on by receiving a logic high state signal through the inverter. Furthermore, the output line becomes the

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logic "low" state and therefore, the signal in the logic "low" state is applied to the bulk of the first NMOS transistor. (See Col. 3, Lines 16-28).

Secondly when the data is in logic "high" state, that is, power source level, Lee teaches that the first NMOS transistor turns on and the second NMOS transistor turns off. Thus the high state potential is accumulated in the output node. Since the potential of input line of the constant voltage means is the logic "high" state, the pull-up transistor turns on and the pull-down transistor turns off by receiving the logic "low" state signal inverted through the inverter. (See Col. 3, Lines 28- 47).

The bias device including the NMOS transistor keeps the potential of the input line in the logic "low" state when the potential of the input line is in the logic "high" state, that is, the power source voltage level, or the ground voltage level does not reach the logic "low" state. In other words, if the potential of the input line does not reach the logic "high" state, the signal is kept in the logic "low" state to be applied to the bulk of the first NMOS transistor. (See Col. 3, Lines 47- 56).

In contrast, as now recited for amended Claim 9 and similarly for amended Claim 10 the presently claimed invention recites at least one delay element; wherein the delay element includes an input signal to be delayed. Amended Claim 1 similarly recites an input signal to be delayed. The present invention also recites for amended Claims 1 and 9-10 a series of at least two delay stages. Each delay stage includes a stack of uniform minimum channel length transistors selected from one of a first conductivity type and a second conductivity type. A gate of each of the transistors in each delay stage are electrically coupled together to form an input in the delay stage.

The present invention further recites that a drain of a top transistor in the stack is coupled to a first reference voltage and a source of a bottom transistor in the stack is coupled to a second reference voltage. A source of the top transistor is electrically coupled to a drain of the bottom transistor in the stage so as to form an output of the

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stage. Additionally, when the input signal to be delayed is in a low state, each transistor of the first conductivity type is active and each transistor of the second conductivity type is inactive. Alternatively, when the input signal to be delayed is in a high state, each transistor of the first conductivity type is inactive and each transistor of the second conductivity type is active.

Lee does not teach or anticipate at least two delay stages. In fact, the intent of Lee is an "off chip" driver and not a delay element as recited by amended Claims 1 and 9-10. The Examiner directs Applicant to FIG. 3 of Lee with specific attention to elements 5 and 7. The Examiner states that elements 5 and 7 constitute a delay stage as recited by the amended Claims 1 and 9-10 of the present invention. However, nowhere does Lee teach a delay stage or for that matter, a series of two delay stages. Additionally, Lee is absent a teaching of uniform minimum channel length transistors. The Examiner only points to FIG. 3 of Lee, without further support, to the pull-up transistor 5 and pull-down transistor 7. However careful reading of Lee does not teach or suggest that the transistors 5 and 7 are uniform minimum channel length transistors. Accordingly, independent claims 1, 9, and 10 distinguish over Lee for at least this reason.

Continuing further, Lee also does not teach or anticipate that a gate of each of the transistors in each delay stage are electrically coupled to form an input in the delay stage. For example, the Examiner points to elements 5 and 7 and these gates are not coupled to receive an input in a delay stage. The gates of transistors 5 and 7 receive different inputs because the gate of transistor 5 is connected to an inverter which is connected to transistor 7. Accordingly, independent claims 1, 9, and 10 distinguish over Lee for at least this reason as well.

For the foregoing reasons, independent claims 1, 9, and 10 as amended distinguish over Lee. Claim 3 depend from independent claim 1 and since dependent claims contain all the limitations of the independent claims, claim 3 distinguish over Lee, as well, and the Examiner's rejection should be withdrawn.

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The Examiner cites 35 U.S.C. § 102(b) and a proper rejection requires that a single reference teach (i.e., identically describe) each and every element of the rejected claims as being anticipated by Lee.¹ The elements in independent claims 1, 9, and 10 of “a series of at least two or more delay stages”; “wherein each delay stage includes a stack of uniform minimum channel length transistors”; and/or “wherein a gate of each of the transistors in each delay stage are electrically coupled together to form an input in the delay stage”, the rejection of Claims 1, 9, and 10 under 35 U.S.C. 102(b) as being anticipated by Lee has been overcome. The Examiner should withdraw the rejection of these claims is not taught or disclosed by Lee. Accordingly, the present invention distinguishes over Lee for at least this reason. The Applicants respectfully submit that the Examiner’s rejection under 35 U.S.C. § 102(b) has been overcome.

(7) Rejections - 35 USC § 103

(7) The Examiner rejected Claim 4 under 35 U.S.C. 103(a) as being unpatentable over Lee U.S. Patent. No. 5,157,219. This rejection is respectfully traversed.

Claim 4 depends from Claim 1, and as discussed above, since dependent claims recite all of the limitations of the independent claim, it is believed that, therefore, Claim 4 already recites in allowable form.

Accordingly, in view of the amendments and remarks above with respect to Claim 1, since Lee either alone or in any combination of the references made of record, does not teach, anticipate, or suggest, the presently claimed invention as recited for Claim 4, Applicants believe that the rejection of Claim 4 under 35 U.S.C. 103(a) has been

¹ See MPEP §2131 (Emphasis Added) “A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.” Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). “The identical invention must be shown in as complete detail as is contained in the ... claim.”

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overcome. The Examiner should withdraw the rejection of these claims.

(11) Citation of Relevant Prior Art

(11) The Examiner cited other relevant prior art. Applicants have reviewed Sato et al. (U.S. Pat. No. 5,602,798), Matsuzaki et al. (U.S. Pat. No. 5,302,871), and Fuji et al. (U.S. Pat. No. 4,700,089) and believe that each of the cited references alone or in any combination, and including any combination with Lee, do not teach, anticipate, or suggest the presently claimed invention. However, additional remarks are given below with respect to Matsuzaki.

Matsuzaki teaches a delay circuit for delaying a signal by a predetermined period of time. In one embodiment, Matsuzaki teaches a delay circuit that includes a first inverter and a second inverter that are connected in cascade between an input terminal and an output terminal. The first inverter includes P-channel MOS FETs and N-channel MOS FETs. The gates of the PMOSs are connected to one another, and the gates of the NMOSs are also connected to one another. The former gates and the latter gates are connected to each other at a node to which the input terminal is connected. The source of the top PMOS is connected to a power supply and the source of the next PMOS is connected to the drain of the top PMOS. Similarly, the source of the next PMOS is connected to the drain of the previous PMOS and this connection pattern continues for the bottom PMOS. As a result, a series five-stage circuit is created. (See Col. 3, Lines 56-68 and Col. 4, Lines 1-7).

The drain of the bottom PMOS is connected to that of the top NMOS. The source of the top NMOS is connected to the drain of the next NMOS and this connection pattern continues for the bottom NMOS, whose source is connected to a power supply. As a result, a series five-stage circuit is created. The first inverter constituted by these PMOSs and NMOSs outputs a signal from its node which is connected at the drains of the bottom PMOS and top NMOS. Matsuzaki also teaches that five resistors can be inserted

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between the five MOS FETs of the first inverter to effectively obtain delay time. (See Col. 4, Lines 7-25).

In the above embodiment taught by Matsuzaki, a second inverter, which includes a PMOS and an NMOS connected in series between the power supplies, is connected between the output node of the first inverter and the output terminal. Both the gates of the PMOS and NMOS of the second inverter are connected to the output node of the first inverter. The second inverter outputs a signal from its output node connected to the drains of the PMOS and NMOS of the second inverter. Additionally, the output node of the second inverter is connected to the output terminal. (See Col. 4, Lines 25- 34).

The second inverter is arranged to shape the waveform of an output signal and is dispensable. More specifically, since a high resistance is added between the power supply and the output terminal in the first inverter, the rise/fall time of an output signal is lengthened, and the waveform of the output signal becomes dull. If the second inverter, whose resistance is low between the power supply and the output terminal, is arranged on the stage posterior to the first inverter, the rise/fall time of the output signal can be shortened, with the result that the dull waveform of the output signal can be improved. (See Col. 4, Lines 34-44).

Matsuzaki also teaches an embodiment with a plurality of inverters, namely first and second inverters, which are similar to the first inverter discussed above. Each inverter includes a plurality of MOS FETs between the power supply and the output terminal and may be connected between the input terminal and the output terminal. The plurality of inverters allows the delay time to be set longer than in the delay circuit according to the above embodiment. Third and fourth inverters are also included, which are similar to the second inverter of the first embodiment. (See Col. 5, Lines 17-50).

Another embodiment taught by Matsuzaki also includes first and second inverters which are similar to the first inverter discussed above. Each inverter comprises a plurality of PMOSs and NMOSs connected between the power supply and the output

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terminal. Terminals are connected between the sources and drains of the PMOSs and NMOSs. Power lines are connected to these terminals allowing the delay time of the two inverters to be controlled. Third and fourth inverters are also included, which are similar to the second inverter of the first embodiment. Matsuzaki also teaches embodiments for controlling the delay time of the inverters, which are comprised of a plurality of PMOSs and NMOSs, by changing the wiring states of the gates of the PMOSs and NMOSs. (See Col. 5, Lines 55-63).

Matsuzaki teaches that the PMOSs and NMOSs constituting the first and second inverters can be designed to have the same size as that of active elements constituting other circuits or that of the single PMOS and NMOS constituting the third and fourth inverters (wave shaping circuit). If the MOS FETs constituting the first and second inverters are designed to have the same gate length as that of MOS FETs of other logic circuits, the rate of variation in delay time in the two inverters can be set equal to that in other logic circuits, even though a mask is shrunk as it is. The channel lengths of the MOS transistors constituting the delay circuits according to the above embodiments are the same as those of MOS transistors constituting peripheral circuits of the delay circuits, such as logic circuits. (See Col. 7, Lines 55-68 and Col. 8, Lines 19-35).

Turning now to the present invention as recited for amended independent Claims 1 and 9-10 recites, among other things, uniform minimum channel length transistors. Amended independent Claim 11 similarly recites minimum channel length transistors. Matsuzaki does not teach, anticipate, or suggest using uniform minimum channel length transistors. In contrast, Matsuzaki only teaches that the PMOSs and NMOSs constituting the delay portion can be designed to have the same size as that of active elements constituting other circuits or that of the single PMOS and NMOS constituting wave shaping circuits. Matsuzaki teaches designing the gate lengths of the delay portion to be the same as that of MOS FETs of other logic circuits so that the rate of variation in delay time in the delay portion can be set equal to that in other logic circuits.

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The use of minimum channel length transistors as recited in the present invention provides many inventions. One of the advantage is enhanced modeling of circuit designs. Another advantage of the present invention is that the minimum channel length transistor, as recited by the present invention, is physically smaller than conventional transistors. Another advantage is that the delay element of the present invention improves production, such as increased chip yield.

Therefore, in view of the remarks above with respect to the present invention and Matsuzaki, Applicant believes that Matsuzaki either alone or in any combination with Lee or any of the references made of record, does not teach, anticipate, or suggest, the presently claimed invention.

(9-10) Allowable/Allowed Subject Matter

(9-10) The Examiner objected to Claims 2 and 5-8, as being dependent on a rejected base claim, but indicated that these claims would be allowable if rewritten in independent form including all limitations of the base claim and any intervening claims.

In view of the amendment and remarks above, Applicants believe that Claims 2 and 5-8 now recite in allowable form. Accordingly, Applicants request that the Examiner withdraw the objection to these claims.

The Applicants wish to thank Examiner Nguyen for indicating that Claims 11-14 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, as discussed above.

Applicant has amended Claim 11 to further recite "wherein when the input is in a low state, each transistor of the first conductivity type is active and each transistor of the second conductivity type is inactive; and wherein when the input to be delayed is in a

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high state, each transistor of the first conductivity type is inactive and each transistor of the second conductivity type is active”.

In view of the amendment and remarks above, Applicants believe that Claims 11-14 now recite in allowable form. Accordingly, Applicants request that the Examiner withdraw the rejection to these claims, as discussed above.

CONCLUSION

The foregoing is submitted as full and complete response to the Official Action mailed October 1, 2004, and it is submitted that Claims 1-14 are in condition for allowance. Reconsideration of the rejection is requested. Allowance of Claims 1-14 is earnestly solicited.

No amendment made was related to the statutory requirements of patentability unless expressly stated herein. No amendment made was for the purpose of narrowing the scope of any claim, unless Applicant has argued herein that such amendment was made to distinguish over a particular reference or combination of references.

Applicants acknowledge the continuing duty of candor and good faith to disclosure of information known to be material to the examination of this application. In accordance with 37 CFR §§ 1.56, all such information is dutifully made of record. The foreseeable equivalents of any territory surrendered by amendment are limited to the territory taught by the information of record. No other territory afforded by the doctrine of equivalents is knowingly surrendered and everything else is unforeseeable at the time of this amendment by the Applicants and their attorneys.

The present application, after entry of this amendment, comprises fourteen (14) claims, including four (4) independent claims. Applicants have previously paid for fourteen (14) claims including four (4) independent claims. Applicants, therefore, believe that a fee for claims amendment is currently not due.

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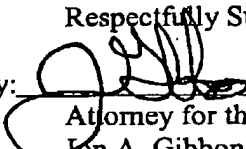
Applicants respectfully submit that all of the grounds for rejection stated in the Examiner's Office Action have been overcome, and that all claims in the application are allowable. No new matter has been added. It is believed that the application is now in condition for allowance, which allowance is respectfully requested.

PLEASE CALL the undersigned if that would expedite the prosecution of this application.

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Respectfully Submitted,

By:


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